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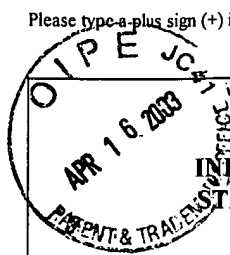


PTO/SB/08A (08-00)

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Sheet	1	of	1	Attorney Docket No.	TI-29298
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Complete If Known	
Application Number	
Filing Date	November 15, 2000
First Named Inventor	Timothy D. Anderson
Group Art Unit	2185
Examiner Name	

U.S. PATENT DOCUMENTS

Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	AA	5,951,679		Anderson, et al.	9/14/99	
	AB					
	AC					
	AD					
	AE					
	AF					
	AG					
	AH					

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FOREIGN PATENT DOCUMENTS

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		Office ³	Number ⁴	Kind Code ² (if known)				
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Exam. Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA		
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Examiner Signature	<i>Shane Senad</i>	Date Considered	9/29/03
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LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Timothy D. Anderson	
				FILING DATE 11/15/00	GROUP

U.S. PTO
09/713731
11/15/00

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE (IF APPROPRIATE)	
	AA	4,626,988	12/86	George	364	200	
	AB	5,579,493	11/96	Kiuchi, et al.	395	375	
	AC	5,600,583	2/97	Bosshart, et al.	364	736.5	
	AD	5,893,142	4/99	Moyer, et al.	711	125	
	AE	5,920,890	7/99	Moyer, et al.	711	144	
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS							
DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION Yes No		
BA							
BB							
BC							
BD							
BE							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
CA	Lee, et al.; <i>Instruction Fetch Energy Reduction Using Loop Caches for Embedded Applications With Small Tight Loops</i> , Int'l Symposium on Low Power Electronics and Design (IEEE, August 10, 1999).
CB	Lee, et al.; <i>Low Cost Branch Folding for Embedded Applications With Small Tight Loops</i> , Int'l Symposium on Microarchitecture (IEEE, November 16, 1999).
CC	
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EXAMINER <i>Shane Jones</i>	DATE CONSIDERED 9/29/03
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